CTAccel Image Processing Accelerator

- **CIP Accelerator solution running on Xilinx Alveo™ U200 Acceleration Card**
- **Throughput Gain: 4 times more than CPU**
- **Latency Reduction: 4 times less than CPU**
- **TCO Reduction: improve the computing density of DC, reduce racks**
- **Software Compatible: ImageMagick, OpenCV, GraphicsMagick, Lepton**

INTRODUCTION

The popularity of smartphones and social networks makes taking and sharing of pictures extremely simple and convenient. As of 2017, there are 2.4 billion active smartphone users worldwide. Images that were taken by smartphone users alone amount to petabytes of data generated every day. Cloud storage has made it easier than ever for mobile phone users to share their pictures on social media and access their pictures from multiple devices. As a result, most smartphone users opt to store their pictures in the cloud. These pictures inevitably end up as image data stored in Internet Data Centers (IDC). As a result, image processing computation including transcoding, thumbnail generation, and image recognition, has generated massive computational workload requirements in the IDC.

The instruction based Von Neumann architecture of CPUs and GPUs have inherent limitations in running image coding and decoding algorithms. Instructions are inherently serial, so there are limitations on utilizing massive data parallelism to improve computational performance.

CTAccel Image Processing (CIP) Accelerator is a Xilinx FPGA based image processing acceleration solution that greatly improves the performance of image processing and image analytics by transferring computational workload from the CPU to the FPGA. CIP's powerful processing capabilities benefit data centers by increasing image processing throughput by 4-6x, reduce computational latency by 4x, and reduce TCO by 3x. CIP redefines data center image processing task with state-of-the-art technologies which utilize massively data parallel algorithm to increase computational performance.

Features and Benefits

High Performance

CIP uses the FPGA as a heterogeneous coprocessor on servers to offload the typical image encoding, processing and decoding workflows from CPU. An x86 server with dual E5-2630 CPU equipped with a single CIP accelerator can increase image processing speed by 4-6x while reducing computational latency by 4x.

Low Power

The CIP accelerator is design as a low power solution. A single accelerator can increase server performance by 4-6x, thus drastically increasing compute density, which translates to less rack space and lower administration cost.

Software Compatibility

CIP is fully compatible with the most popular open source image processing software:
OpenCV, ImageMagick , GraphicsMagick, and Lepton The perfect integration of the mainstream image processing software allows users to migrate seamlessly from software-based implementation to CIP.

Low Maintenance

CIP employs advanced Xilinx FPGA Partial Reconfiguration (PR) technology. The computation cores can be upgraded and reconfigured remotely to maximize the performance for custom usage scenario. PR technology allows fast and easy context switch of accelerator functionality without rebooting the server.

Accelerated Functions
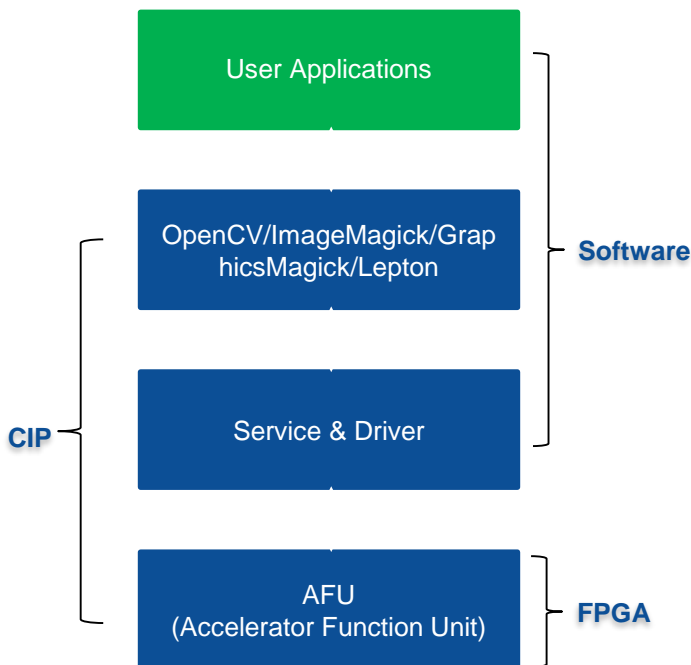
JPEG to Lepton
JPEG decode + resize

Use Case

1. Thumbnail Generation
2. Resize
3. Watermark
4. Brightness/Contrast
5. Sharpen
6. Maincolor
7. Image storage

Test Environment

- CPU : 2x Intel(R) Xeon(R) CPU
- E5-2630 v2 @ 2.60GHz
- RAM : 128GB
- OS: CentOS Linux release 7.2.1511
- Kernel version: 3.10.0-327.36.2.el7.x86_64
- FPGA: Xilinx UltraScale+
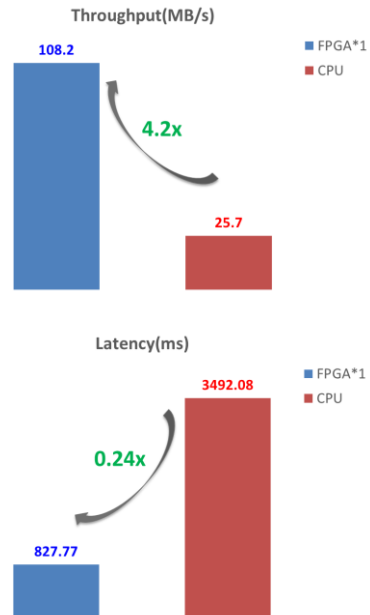- Platform: SDAccel 2017.4

Software Architecture

User Applications

OpenCV/ImageMagick/GraphicsMagick/Lepton — **Software**

Service & Driver

AFU (Accelerator Function Unit) — **FPGA**

CIP

Performance

Function-1: JPEG to Lepton

Throughput(MB/s)
- FPGA*1: 108.2
- CPU: 25.7
- 4.2x

Latency(ms)
- CPU: 3492.08
- FPGA*1: 827.77
- 0.24x

Function-2: JPEG decode + resize

Throughput(MB/s)
- FPGA*1: 680.3
- CPU: 102.9
- 6.6x

Latency(ms)
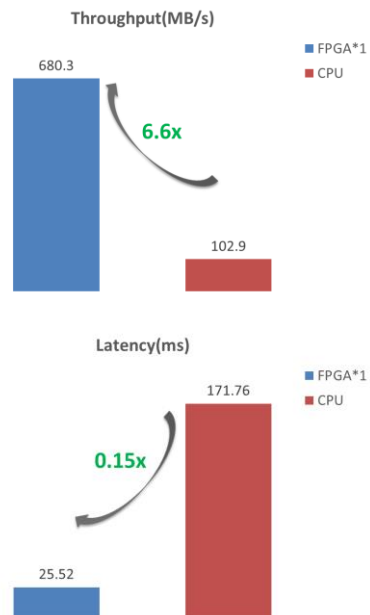- CPU: 171.76
- FPGA*1: 25.52
- 0.15x

About CTAccel Ltd

- Founded in Mar, 2016
- Based in Hong Kong & Shenzhen
- Core team members from: CUHK、HKUST、FDU、CAS
- Focus on FPGA-based processing and acceleration
- US Patent
- Core value of our company: Quality & Innovation

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CTACCEL
Accelerated Computing